CLAIMS

Please amend the claims as follows:

1-10. (cancelled)

11. (previously presented) A semiconductor device comprising:

a stacked gate structure;

a first p-type region of substrate disposed adjacent to a first side of the stacked gate structure;

a first n-type region of substrate disposed adjacent to a second side of the stacked gate structure; and

a second n-type region of substrate disposed adjacent to the first and second regions, the second n-type region including p-type dopants at a concentration corresponding to the first p-type region.

12. (previously presented) The semiconductor device of claim 11, wherein the second n-type region further comprises n-type dopants at a concentration sufficient to over compensate for the p-type dopants.

13. (previously presented) The semiconductor device of claim 11, wherein the stacked gate structure is located in a core portion of an integrated circuit device.

14. (previously presented) The semiconductor device of claim 11, wherein the stacked gate structure, p-type region, and the first and second n-type regions form a memory cell, and the semiconductor device comprises a plurality of the memory cells.

15. (previously presented) The semiconductor device of claim 14, wherein the memory cells are organized into rows and columns.

16. (currently amended) The semiconductor device of claim 15, wherein [[the]] p-type regions are disposed between memory cells within a row and [[the]] first n-type regions are disposed between memory cells within a column.

17-25. (cancelled)